REMARKS

Claims 1-32 are pending in the application. Claims 1-32 have been examined. Claims 1-2, 5-9, 11-15, 20, 22-25, 27-28 and 30-32 are rejected and claims 3-4, 16-19, 21, 26, and 29 are allowable. Claim 10 is objected to. Claims 1-2, 5-7, 9-15, 20, 22-25, 27, 28, 30-32 have been amended to more clearly define the invention. Reconsideration and allowance of the claims are respectfully requested.

THE CLAIMS

Allowable Claims 3-4, 16-19, 21, 26 and 29

Applicants note with appreciation the indication of allowable claims 3-4, 16-19, 21, 26, and 29.

Objection to Claim 10

Claim 10 is objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form. Claim 10 has been amended to include the limitations of base claim 9.

Objection Under 35 U.S.C. §132

The amendment filed on 6/23/03 is objected to under 35 U.S.C. §132 because claim 7 contains materials deemed not supported by the original disclosure. Claim 7 has been amended to include the limitation "check a predetermined number of most significant bits (MSBs) of the exponent of the preliminary result to determine whether the preliminary result falls within the plurality of ranges of denormalized values." The materials supporting this limitation are found on page 24, lines 9-13, of the specification.

Rejection of Claims 1-2, 5-7, 20, 22-24, 27-28, and 30-32 Under 35 U.S.C. §102(b)

Claims 1-2, 5-7, 20, 22-24, 27-28, and 30-32 stand rejected under 35 U.S.C. §102(b) as being anticipated by Hirose *et al.* (U.S. Patent No. 4,839,846). The rejection states that Hirose discloses a floating-point unit configurable to perform floating-point operations in FIGS. 7-8. The floating-point unit receives and processes one or more input operands (60) to provide a preliminary result (70), determines whether the preliminary result falls within one of a plurality of ranges of values (based on the least

significant bits in FIG. 4A), and sets the preliminary result to one of a plurality of set values if the preliminary result falls within one of the plurality of ranges of values (col. 2, lines 35-48).

Hirose Reference

Hirose describes in FIG. 8 a method of performing floating-point add/subtract operation by the floating-point unit in FIG. 7 (see col. 3, lines 9-10). For a floating-point add/subtract operation, the difference between the exponents of two operands is first determined (60), the mantissa of the smaller operand is shifted to the right by the difference between the exponents, and the two mantissas are added or subtracted (70) (see col. 2, lines 34-38). The result of the add/subtract operation may be a number that is not normalized. The operation result is thus normalized and then rounded. The normalization is performed by shifting the mantissa to the left so that the most significant bit (MSB) of the mantissa is a one ('1') and decrementing the exponent accordingly. The rounding is performed based on (a) the least significant bit (LSB) of the mantissa after the normalization, (b) three bits to the right of the LSB, which are referred to as the "guard" bit, "round" bit, and "sticky" bit, as shown in FIG. 3, and (c) the rounding mode selected for use. Four different rounding modes are given in FIGS. 4A through 4D. Whether or not the mantissa should be rounded up is determined based on these four mantissa bits and the selected rounding mode. If a round-up is performed, an overflow in the mantissa may occur, as shown in FIG. 16C. In this case, the mantissa is shifted right by one bit to obtain a normalized mantissa, as shown in FIG. 16D, and the exponent is incremented by one (see col. 4, lines 65-68).

Present Invention

Claim 1 of the present invention, as amended, recites:

"A floating-point unit (FPU) configurable to perform floating-point operations, comprising:

an operand processing section operative to, for each floating-point operation, receive and process one or more input operands to provide a preliminary result comprised of a mantissa and an exponent; and

an operand flush section coupled to the operand processing section and operative to check at least the exponent of the preliminary result to determine whether the preliminary result falls within one of a plurality of ranges of denormalized values between zero and a minimum normalized floating-point number, a_{min}, and

set the preliminary result to one of a plurality of set values if the preliminary result falls within one of the plurality of ranges of denormalized values, wherein each set value is defined by a particular exponent value and a particular mantissa value."

Applicants submit that claim 1 is not anticipated by Hirose for at least the following reasons (in additional to those noted in the amendment filed on 6/23/03).

First, Hirose does not describe nor suggest an operand flush section operative to "check at least the exponent of the preliminary result to determine whether the preliminary result falls within one of a plurality of ranges of denormalized values between zero and a minimum normalized floating-point number." The section of Hirose indicated as disclosing this feature (FIG. 4A) actually describes checking a sign bit and four mantissa bit (and NOT the exponent) to determine whether or not to round up.

Second, Hirose does not describe nor suggest "ranges of denormalized values." The ranges of values noted in the rejection for FIGS. 4A through 4D of Hirose are for the four mantissa bits.

Third, Hirose does not describe nor suggest the operand flush section operative to "set the preliminary result to one of a plurality of set values if the preliminary result falls within one of the plurality of ranges of denormalized values, wherein each set value is defined by a particular exponent value and a particular mantissa value." In Hirose, the round-off or round-up operation is performed on the mantissa. Hirose "rounds" the mantissa and does not "set" the exponent or the mantissa.

For at least the above reasons, Applicants submit that claim 1 of the present invention is not anticipated by Hirose.

Independent claims 20, 23, 27, and 30-32 each recite features similar to that described above for claim 1. Applicants submit that these independent claims are not anticipated by Hirose for reasons similar to those noted above for claim 1.

Claims 2 and 5-7 are dependent on claim 1, claim 22 is dependent on claim 20, claim 24 is dependent on claim 23, and claim 28 is dependent on claim 27. These claims are not anticipated by Hirose for at least the reasons noted above for their base claims. These dependent claims may further recite additional features not described or suggested by Hirose.

Accordingly, the §102(b) rejection of claims 1-2, 5-7, 20, 22-24, 27-28, and 30-32 should be withdrawn.

Rejection of Claims 9, 11-15 and 25 Under 35 U.S.C. §103(a)

Claim 9, 11-15 and 25 stand rejected under 35 U.S.C. §103(a) as being obvious over Hirose *et al.* (U.S. Patent No. 4,839,846) in view of Mansingh (U.S. Patent No. 6,199,089). With regard to claim 9, the rejection states that Hirose discloses the mantissa processing section and Mansingh in FIG. 3A discloses the exponent processing section. The rejection further states that unit **208** in FIG. 3A of Mansingh sets the preliminary result exponent to first or second exponent values if the result of a floating-point operation falls within first and second ranges of values.

Mansingh Reference

Mansingh describes in FIG. 3A a floating-point unit **100** with two operation units **200** and **300** (see FIG. 1). Operation unit **200** is used to perform addition or subtraction when the absolute value of the difference between the exponents of the two operands is greater than one (col. 2, lines 62-66). Operation unit **300** is used to perform subtraction when the absolute value of the exponent difference is less than or equal to one (col. 3, lines1-4)). Decision unit **208** determines whether (a) the absolute value of the exponent difference is less than or equal to one ('yes' from unit **208**) in which case operation unit **300** is used or (b) the absolute value of the exponent difference is greater than one ('no' from unit **208**) in which case operation unit **200** is used.

Present Invention

Claim 9 of the present invention, as amended, recites:

"A floating-point unit (FPU) configurable to perform floating-point operations, comprising:

a mantissa processing section operative to, for each floating-point operation,

receive and process one or more mantissas for one or more input operands for the floating-point operation to provide a preliminary result mantissa,

set the preliminary result mantissa to a first mantissa value if a preliminary result for the floating-point operation, comprised of the preliminary result mantissa and a preliminary result exponent, is within a first range of denormalized values between zero and a minimum normalized floating-point number, a_{min}, and

set the preliminary result mantissa to a second mantissa value if the pre result is within a second range of denormalized values between zero and the minimum normalized floating-point number; and

an exponent processing section operative to

receive and process one or more exponents for the one or more input operands for the floating-point operation to provide the preliminary result exponent,

set the preliminary result exponent to a first exponent value if the preliminary result is within the first range of denormalized values, and

set the preliminary result exponent to a second exponent value if the preliminary result is within the second range of denormalized values."

Applicants submit that claim 9 is patentable over Hirose in view of Mansingh for at least the following reasons.

First, neither Hirose nor Mansingh describe the condition "if a preliminary result for the floating-point operation, comprised of the preliminary result mantissa and a preliminary result exponent, is within a first range of denormalized values between zero and a minimum normalized floating-point number." Instead, Hirose uses four mantissa bits to determine whether to round-off or round-up. Mansingh determines whether the absolute difference between two exponents, e_a and e_b, is less than or equal to one (see column 3, lines 36-37). Applicants submit that the condition for whether the preliminary result for the floating-point operation is within a range of denormalized values cannot be made by checking four mantissa bits or the absolute exponent difference.

Second, neither Hirose nor Mansingh describe setting the preliminary result mantissa and preliminary result exponent to specific (first or second) mantissa and exponent values, respectively. Instead, Hirose "rounds" (and does not "set") the mantissa. Mansingh "swaps" the position of the mantissas (in unit 214) and "swaps" the position of the two exponents (in unit 215 located to the left of unit 206) based on the comparison result from unit 216.

For at least the above reasons, Applicants submit that claim 9 of the present invention is patentable over Hirose in view of Mansingh.

Independent claim 13 recites features similar to that described above for claim 9 and is patentable for reasons similar to those noted above for claim 9. Claims 11-12 are dependent on claim 9, claims 14-15 are dependent on claim 13, and claim 25 is dependent on claim 23. These claims are patentable over Hirose in view of Mansingh for at least the reasons noted above for their base claims.

Accordingly, the §103(a) rejection of claims 9, 11-15 and 25 should be withdrawn.

CONCLUSION

Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (650) 289-0600.

Respectfully submitted,

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